5. Introduction to and Advances in 2.3D Fan-Out Wafer Level Packaging (FO-WLP)

Course Leader: Beth Keser - Zero ASIC

Course Description:
Fan-out wafer level packaging (FO-WLP) technologies have been developed across the industry over the past 20 years and have been in high volume manufacturing for over 16 years. FO-WLP has matured enough that it has come to a crossroads where it has the potential to change the electronic packaging industry by eliminating wirebond and bump interconnections, substrates, leadframes, and the traditional flip chip or wirebond chip attach and underfill assembly technologies across multiple applications. After scale-up and high-volume manufacture of simple single-chip Fan-Out Wafer Level Packaging (FO-WLP) solutions by companies like Qualcomm and Infineon, now many premier semiconductor companies and OEM's have adopted Advanced Fan-Out structures including Apple, AMD, MediaTek, and HiSilicon. These companies are leveraging foundry technologies like InFO offered by TSMC as well as OSAT solutions from ASE, Amkor, SPIL, PTI, and DECA.

The introductory portion of this course will cover the advantages of FO-WLP, potential application spaces; package structures available in the industry; materials, equipment and process challenges; and reliability. The advanced topics will cover potential application spaces, advanced package structures available in the industry, adopting 2.3D chips first and chips last fan-out technology for chiplets, technology roadmaps, and benchmarking.

Course Outline:

1. Definitions and Advantages
2. Applications
3. Early Package Structures
4. Materials
5. Equipment
6. Design Rules and Reliability
7. Advanced Applications Including Chiplets
8. Package Structures Including Advanced FO technologies
9. Technology Roadmap
10. Panel Challenges
11. Benchmarking

Who Should Attend:
Engineers and managers responsible for advanced packaging development, package characterization, package quality, package reliability and package design should attend this course. Suppliers who are interested into supporting the materials and equipment supply chain should also attend. Both newcomers and experienced practitioners are welcome.

Bio: Beth Keser, Ph.D., a recognized global leader in the semiconductor packaging industry with over 27 years of experience, received her B.S. degree in Materials Science and Engineering from Cornell University and her Ph.D. from the University of Illinois at Urbana-Champaign. Beth's excellence in developing revolutionary electronic packages for semiconductor devices has resulted in 49 patents and patents pending and over 50 publications in the semiconductor industry. Previously, Beth had led fan-out and fan-in wafer level packaging

development and product qualification teams at Motorola, Freescale, Qualcomm, and Intel. In 2019, Beth published Advances in Embedded and Fan-Out Wafer-Level Packaging Technologies (Wiley) and in 2021 released her second book Embedded and Fan-Out Wafer and Panel Level Packaging Technologies for Advanced Application Spaces: High Performance Compute and System-in-Package (Wiley).

Beth was awarded the 2021 IEEE EPS Exceptional Technical Achievement Award for seminal contributions and leadership in FO-WLP. Beth was General Chair of ECTC in 2015 and has been a member of the ECTC Packaging Technology Subcommittee for over 20 years. Currently, Beth VP of Manufacturing at the chiplet start-up Zero ASIC, an IEEE Fellow and IEEE EPS Distinguished Lecturer.